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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,044	01/18/2006	Chris Wyland	US03 0251 US2	3935
24738	7590	10/31/2006	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			RODELA, EDUARDO A	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/565,044	WYLAND, CHRIS
	Examiner	Art Unit
	Eduardo A. Rodela	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 18 August 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 2-11 and 13-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 13, 15 and 16 is/are allowed.
 6) Claim(s) 2-11 is/are rejected.
 7) Claim(s) 14 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 18 August 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the...

- a.) **plurality** of grounding pads, signal pads, and power pads (of claim 4),
- b.) **plurality** of grounding pads (claim 6),

...must be shown or the feature(s) canceled from the claim(s).

No new matter should be entered. The drawings do not show more than one grounding pad [380], and show two generic "pad landings" [115,215,315], but do not show a plurality of power pads and signal pads.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: As recited on page 5, lines 18-20, imply that the conductive bonds 350a and 350b are disposed on the die, but as Figure 4 shows the conductive bonds 350a and 350b are not on the die [330], but on the substrate [310].

Also, the disclosure is objected to because of the following informalities: As recited on page 5, 350a and 350b are called "conductive bonds (lines 16 and 17)" and "ground traces (line 27)." As 350a and 350b appear to be solder balls or some sort of bonding material, they would more correctly be called "conductive bonds."

Appropriate correction is required.

Claim Objections

Claim 4 is objected to because of the following informalities: The semiconductor chip is repeatedly referred to as the "the integrated circuit the semiconductor device die". Appropriate correction is required. All of the dependent claims must refer to the semiconductor chip in a consistent manner, e.g. the by the same name.

Claim 14 is objected to because of the following informalities: The angle claimed is unclearly labeled as "90o", for clarification purposes, it is suggested that it should be replaced with "90 degrees".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 states, "the grounding arch is coupled to at least one **grounding location on the integrated circuit device**, wherein the grounding location includes, the grounding trace and grounding pads." However, the specification and drawings (Figure 4) disclose that the grounding traces 340a, 340b, 350a, and 350b are located on the substrate [310] and not on a grounding location [380] on the integrated circuit device [330].

Claim 6 recites the limitation " the grounding arch is coupled to at least one **grounding location on the integrated circuit device**, wherein the grounding location includes, the grounding trace and grounding pads " in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to where the grounding trace is since it is originally said to be surrounding the integrated circuit (lines 4 and 5 of claim 1).

Although an attempt to clarify the claim language was made by the applicant, claim 4, which claim 6 depends, still has the "reference trace" as surrounding the integrated circuit, lines 4 and 5 of claim 4. The specification labels the conductive path [Figure 4: 350c] from the grounding arch [370] to the ground pad [380] on the semiconductor chip [330], a "conductive bond" on lines 19 and 20 on page 5 of the specification. This issue still renders claim 6 as indefinite. This discrepancy must be addressed.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 11 contains the trademark/trade name TEFLON. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe the type of dielectric used on the grounding arch, and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 2003/0116836) in view of Baudouin et al. (US 6,373,127).

Regarding claim 4, Huang et al. disclose in Figure 2, an integrated circuit device comprising: a semiconductor device die [210] having a plurality of grounding pads

[212b], signal pads [211c], and power pads [212a]; and a package [200] for mounting the integrated circuit the semiconductor device die [210] and including a conductive path having at least one reference trace [201a-c] surrounding the integrated circuit the semiconductor device die [210] and having a grounding arch [231,232] disposed over the semiconductor device die [210], and wherein the grounding arch [231,232] is comprised of metal tape [paragraph 0029]. Huang et al. do not disclose that the grounding arch is laminated with a dielectric material. Baudouin et al. do disclose in Figure 7, the use of a metal conductor [774] used to electrically connect a chip [71] to a substrate [771], which is laminated with a dielectric material [773]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the dielectric material of Baudouin in the metal conductor of Huang in order to mitigate the possibility of electrical short circuiting with nearby conductors [column 6: lines 10-20].

Regarding claim 2, Huang and Baudouin disclose the integrated circuit device of claim 4. In addition, Huang et al. disclose wherein the reference trace [201b] is coupled to a ground reference [paragraphs 0018,0024].

Regarding claim 3, Huang and Baudouin disclose the integrated circuit device of claim 4. In addition, Huang disclose wherein the grounding arch [231,232] has an area [portion 232] comparable [paragraph 0031] to the area of the semiconductor device die [210].

Regarding claim 5, Huang and Baudouin disclose the integrated circuit device of claim 4. In addition, Huang et al. disclose in Figure 2, wherein the grounding arch

[231,232] has a predetermined thickness thereby providing sufficient structure preventing electrical contact [shown in figure] between the grounding arch [231,232] and wire bonds [243].

Regarding claim 6, Huang and Baudouin disclose the integrated circuit device of claim 4. In addition, as it is understood by the examiner, Huang et al. disclose in Figure 2, wherein the grounding arch [231,232] is coupled to at least one grounding location [212b] on the integrated circuit device [210], wherein the grounding location includes, a trace [233] and the grounding pads [212b] on the semiconductor device die [210].

Regarding claim 7, Huang and Baudouin disclose the integrated circuit device of claim 6. In addition, Huang et al. disclose in Figure 2, wherein the grounding location further includes a location about a center region [shown to be centrally located] on the semiconductor device die [210].

Regarding claim 8, Huang and Baudouin disclose the integrated circuit device of claim 5. In addition, Huang et al. disclose in Figure 2, wherein the grounding arch comprises conductors of a highly conductive material such as copper [paragraph 0029].

Regarding claim 9, Huang and Baudouin disclose the integrated circuit device of claim 5. In addition, Huang et al. disclose in Figure 2, wherein the highly conductive material is in a form of a solid tape [paragraph 0029].

Regarding claim 10, Huang and Baudouin disclose the integrated circuit device of claim 6. In addition, Baudouin et al. disclose wherein metal with laminated dielectric is coupled at the connection points with solder/eutectic metal bond [column 6: lines 10-20, solder is a type of eutectic].

Regarding claim 11, Huang and Baudouin disclose the integrated circuit device of claim 4. In addition, Baudouin et al. disclose wherein the dielectric material is solder mask [column 6: lines 10-20, it is noted that polymer based dielectrics are widely used in soldermasks, such as shown in US 4,847,114, column 10: lines 20-35, “A copper laminate used in the art for printed circuit manufacture was drilled, imaged, and etched, to form a circuit in the conventional manner. A permanent soldermask was applied by screen printing, covering all the circuitry, except for the pads and the through-holes. The soldermask used in this case was based upon a complex epoxy polyacrylate polymer, which is typical of the screen inks used in the art.”].

Allowable Subject Matter

Claims 13, 15, and 16 are allowed.

Claim 14 would be allowable once the claim objection is addressed (see the Claim Objections section of the Office Action).

The following is an examiner’s statement of reasons for allowance: The method for controlling impedance of bond wires in packaging a semiconductor device die in a package as recited in the claim 13 of the instant invention fail to be taught by the prior art cited of interest. Huang shows a semiconductor device die in a package but fails to teach the specific characteristic of the structure recited in the claims of the instant invention e.g. the method including the “rotating the package a pre-determined amount; and providing an additional ground arch”.

Fax / Telephone Information

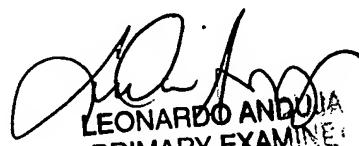
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eduardo A. Rodela
Examiner

ER



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PRIMARY EXAMINE